Investigating the Diamond Buffer Input Stage in a Current Feedback Audio Amplifier:

Does it Operate in Class A, B or Class AB Mode?

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October, 2017

Claim: The CFA Diamond Buffer Stage Operates in Class B

There is a persistent assertion by small group of amplifier design practitioners that the diamond buffer (hereinafter referred to as 'DB') input stage of CFA audio amplifier[1] operates in class B or class AB mode, the most recent in the June issue of AudioXpress by M. Kiwanuka, from which I quote

> *" . . . . Therefore, contrary to the comments by Andrew C. Russell in his article "CFA vs VFA: A Short Primer for the Uninitiated," the voltage amplifier of Figure 1 is of no use whatsoever in audio frequency applications because its significantly low major loop gain (compared with that generated by the circuit shown in Figure 6) is insufficient to satisfactorily mitigate the non-linearity generated by its forward path. The performance of the circuit shown in Figure 1 is further degraded by the fact that its complementary common-emitter input stage operates in Class-B. It's bad enough that crossover distortion arising from Class-B operation has to be tolerated in the output stage, but extending it to the input stage as well is downright perverse, at least as far as audio frequency applications are concerned. . . . "*

(Note: Mr. Kiwanuka is referring to the Figure 1 in his article in AudioExpress)

In plain English, the claim being made is that the complementary diamond buffer ('DB') front end in a CFA runs in class B or class AB. Since the class AB output stage contributes *most of the distortion* in a well-designed VFA amplifier, the logic of this claim is that CFA amplifiers have two stages – the input and the output – running in class B or class AB mode, so they must be worse with regard to distortion and, subjectively, audibly worse than competing topologies. Further, the claim is that the situation is compounded by the lower loop gains one encounters in CFA's, thus making them unsuitable for audio applications.

Class B Operation

Let's remind ourselves what class B/AB operation looks like with this LTSpice sim snap shot below, and why in a sub-optimally designed system it is so objectionable.

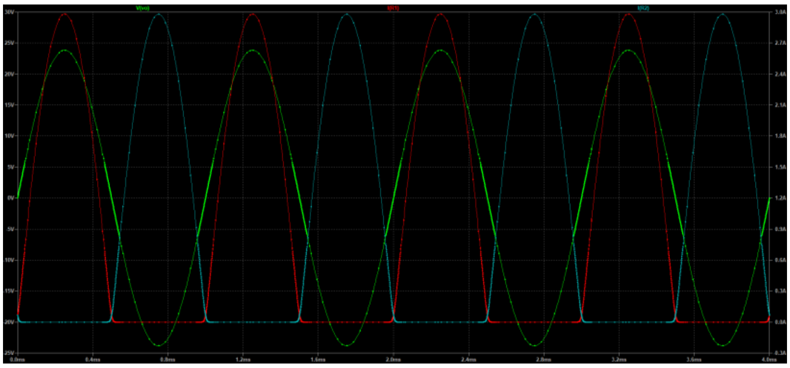

Figure 1 - Class AB Output Stage Waveforms

[1] The discussion in this document will centre around discrete audio power amplifiers and not IC operational amplifiers. In IC CFA operational amplifiers, the input stage may well operate in class B or AB mode as a potential power saving feature. However, discrete audio power amplifiers suffer none of the power constraints imposed on IC devices and thus in the DB level shifter transistors

It is clear from Fig. 1 that the current supplied into the load (red trace) only flows over one half the full cycle of the load voltage (green trace), whilst the aqua trace flows over the other half.

In a class AB EF1 output stage that is correctly biased, using modern sustained beta devices, you can expect about 350ppm *open loop* distortion at 1 kHz with a *single pair* of output devices driven from voltage source delivering 75 watts peak into an 8 ohm load. The spectral plot of such a configuration is shown below – remember this is in the open loop condition.

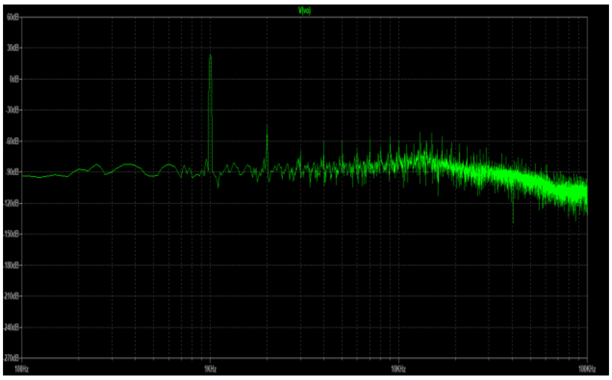

Figure 2 - spectral plot - correctly biased class AB OPS – c. 350ppm at 1 kHz 75 Watts into 8 ohms OPEN LOOP

Paralleling output devices, and ensuring there is sufficient bias such that there are no conduction discontinuities, will result in a decrease in open loop distortion by a factor of ~ √2 for each additional pair. As an aside, you see why big muscle amps with numerous paralleled output devices often feature much lower distortion than smaller amplifiers using only 1 output pair.

If we *under bias the output stage* so that there is a distinct dead zone between the two halves of the output stage where neither is delivering any current into the output load, there is a significant increase in distortion of the most objectional kind with lots of high order harmonics and this is shown in Fig. 3 below.

The open loop distortion in the plot below, with the conduction crossover discontinuity, is about 0.35%, so about 10x higher than that is the previous plot.

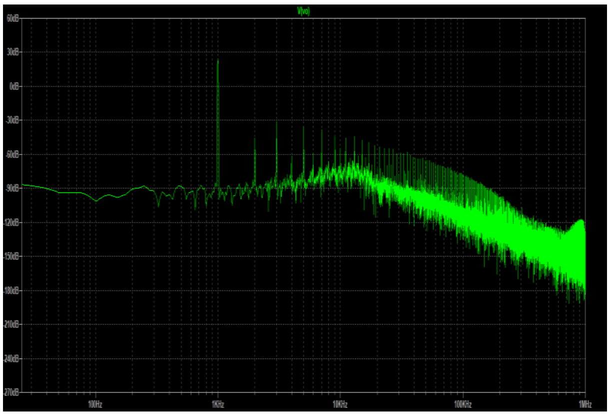

Figure 3 - Underbiased class AB OPS - otherwise same conditions as Fig 2 results in 0.35% distortion

It is clear then why the output stage bias conditions in a class AB amplifier are so important, and further, why if an amplifier had a class B/AB input stage with a conduction discontinuity it would be a problem.

So, this is a legitimate concern, but is it founded on a clear understanding of the operating conditions in a CFA DB front end? Lets investigate using the 100 Watt nx-Amplifier, a classic CFA amplifier design with a class AB output stage and a DB input stage.

CFA Diamond Buffer Configurations

Fig. 4 shows some typical CFA amplifier DB input stage configurations. There are many variations on the themes shown – for example the level shifter transistors (this is the second pair of transistors in each circuit) often drive a cascode stage, allowing the use of low voltage, high hFe devices in this location. The front-end buffers in the examples shown are fed via a 10 k reference resistor from a 10 V zener reference to provide a nominal ~1 mA reference current. Designers often replace these reference resistors with current sources.

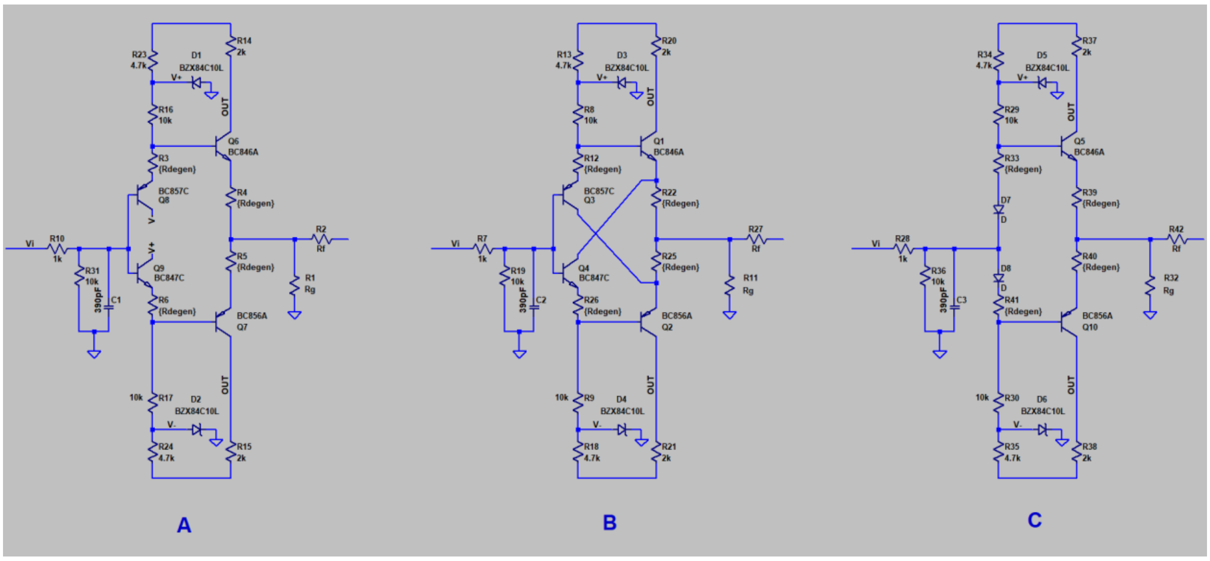

Figure 4 - Some examples of DB configurations

The hifisonix DIY CFA amplifier designs (sx-Amplifier, nx-Amplifier) and the [Ovation High Fidelity] commercial amplifiers (Model 1701, Model 1707 and Model 1721) all use the variants A and B DB shown in Fig. 4. In A above, which we will use for the rest of this discussion, R4 and R5 are the summing junction degeneration resistors, through which we will measure the standing current to determine the collector output current operating class of the front end DB. Note that in Fig 4 A through C, we have shown Rdegen as being the same for the front end buffer transistors (Q8/Q9 in A), and for the level shifter transistors (Q6 and Q7 in A). In practical designs, these may be different and this of course depends on design specifics and the choices and tradeoffs the designer makes. In my designs, these resistors are always 150 Ohms.

The nx-Amplifier model is shown in Fig. 10 while Fig. 5 shows the summing junction currents with the degeneration resistors (in this case) set to 150 Ohms. The nominal output current is 1 mA and the imbalance between the two halves is about 30uA peak and due to Vbe mismatches in the input devices and slightly different gains in each half of the TIS stage which can be removed by matching devices and/or providing offset adjustment. As can be seen, under steady state sine wave input/output conditions, at 100W full power, the DB remains solidly in class A – neither of the level shifter's collector currents is off at any time.

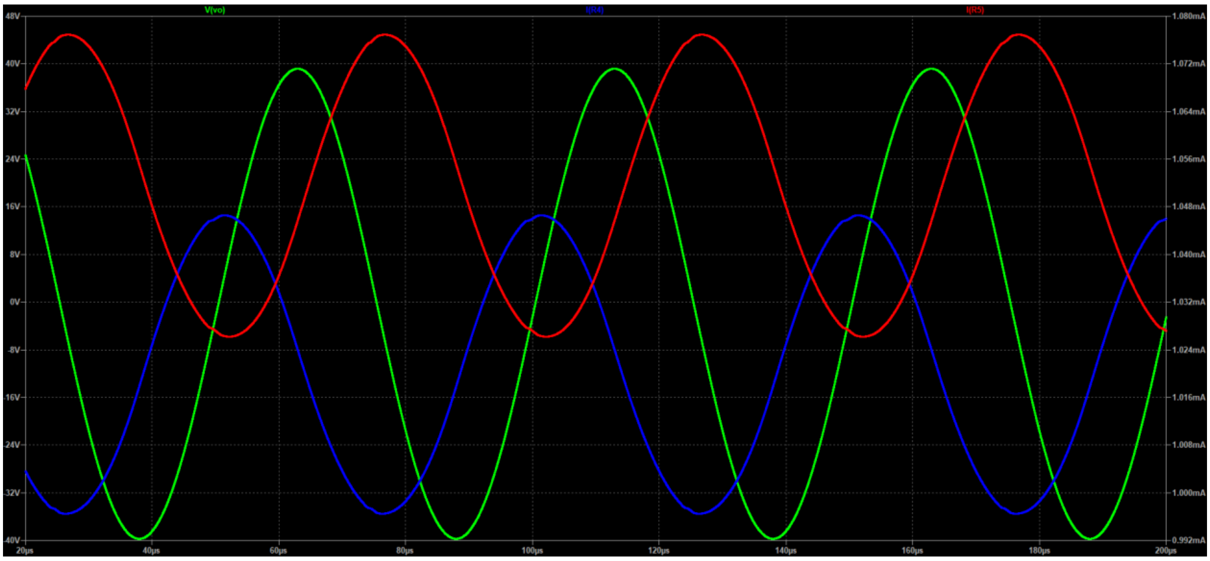

Figure 5 - DB summing junction current with a 40V peak sinew wave output voltage (8 Ohm load). The green trace is the amplifier output voltage shown for reference.

Now we should take a look at the situation with a *fast rise time square wave* stimulus. This is somewhat analogous to feeding a step function into a VFA such that one half of the input LTP is turned OFF or *approaches* turn-off and the amplifier is driven into slewing – the cause of potential TIM or SID during normal audio signal levels in 1970's solid state VFA amplifiers and a phenomena Prof. Matti Otala described in a number of papers at the time (however, see Dr. Bruno Putzeys' refutation of Prof. Otala's conclusions in Part 1 and Part 2).

For this test, we will use a 25 kHz square wave with implausibly fast rise/fall times for audio – say 10 ns which is 200 x faster than the absolute worst case audio signal rise time of 2 us corresponding to a ~175 kHz bandwidth (remember, a CD's bandwidth is just a shade over 20 kHz, so we are being *very conservative* here). Let's also REMOVE the front-end band limiting filter so that the input stage is fully exposed to these fast rise/fall times. The resultant plot is shown in Fig. 6 below.

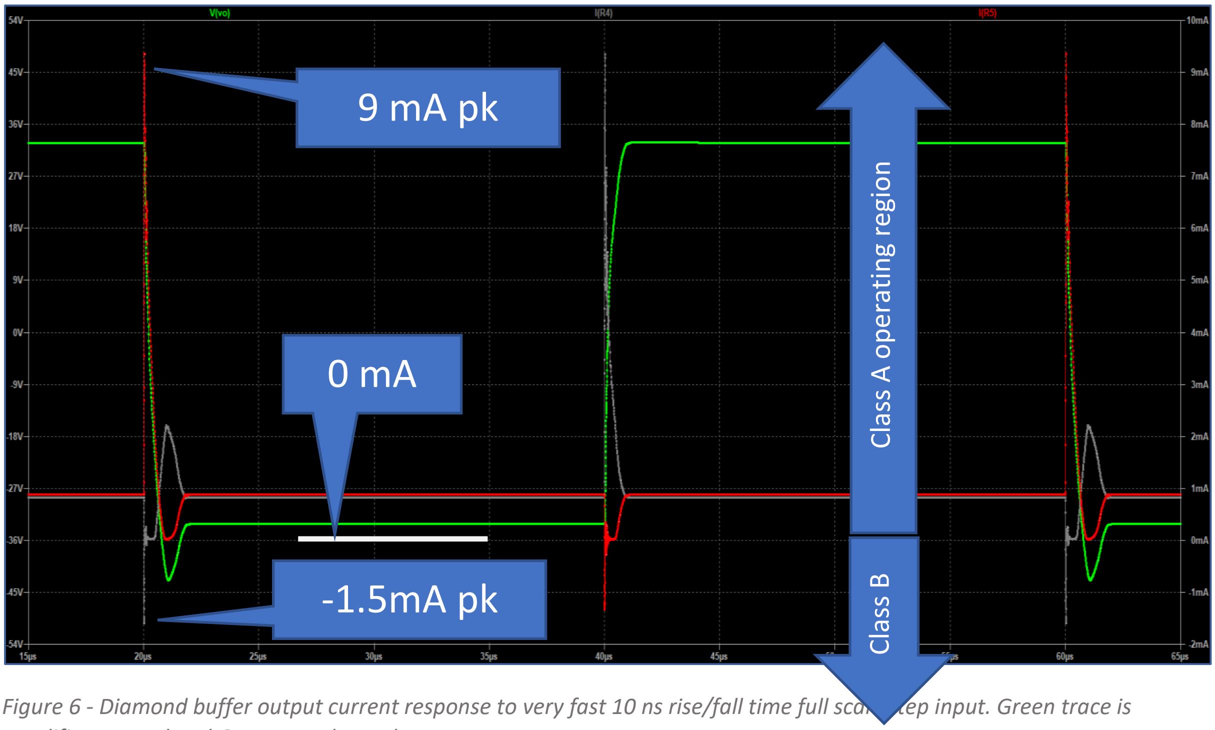

Figure 6 - Diamond buffer output current response to very fast 10 ns rise/fall time full scale step input. Green trace is amplifier Vo, Red and Grey R4 and R5 Rdegen currents

The plot below (Fig. 7) zooms in on the degeneration resistor currents and indeed, we see that under these conditions, the DB output stage conduction is discontinuous at the signal edges. Note however, the input signal is a ±1V pk~pk square wave with 10 ns rise/fall times. We will <u>not ever</u> encounter these conditions in with a normal audio signal input.

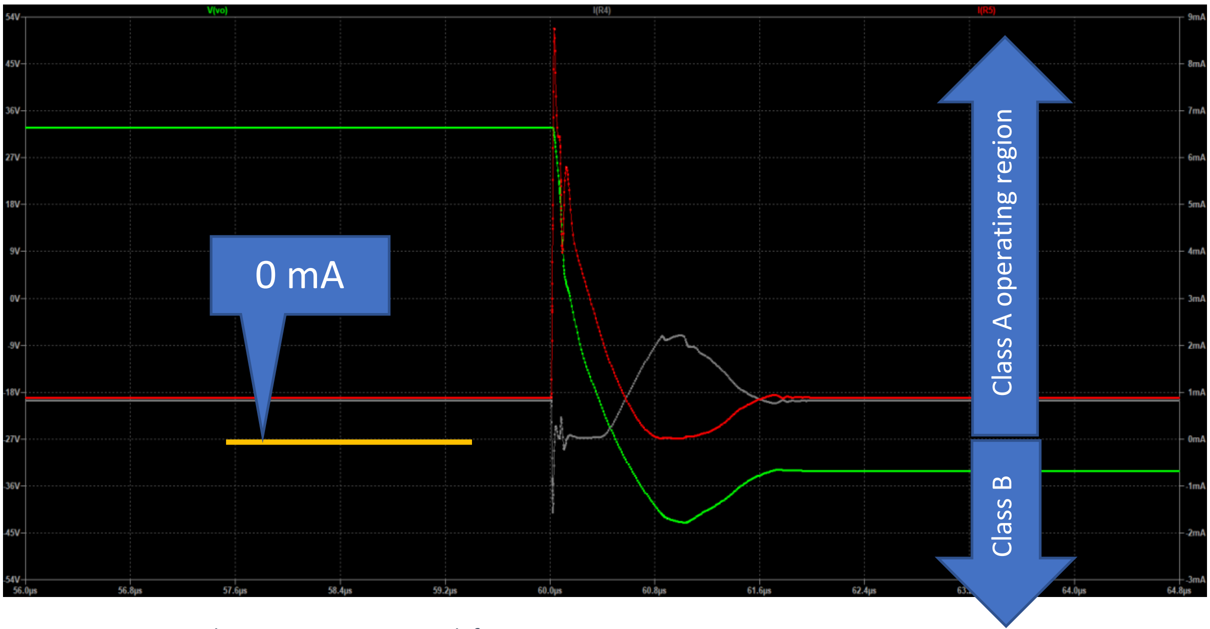

Figure 7 - Zoom into the DB output current with fast step input

Next, we *increase the input signal rise/fall times* to 2 uS – still about 10x faster than we will encounter from any music signal – and we get the plot in Fig. 8 below.

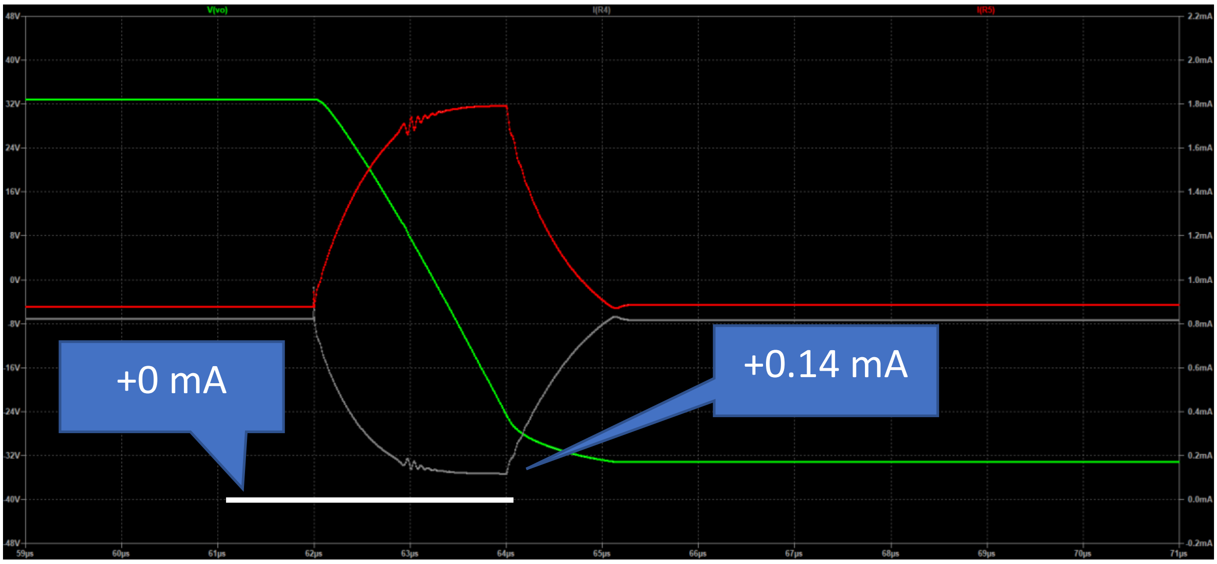

Figure 8 - DB output current response to a 2 us step input

The DB output stage now *remains in class A* over the full input operating range of +-1V with the input signal 2 us rise/fall times for 32 V peak output which corresponds to a bandwidth of 175 kHz. This holds true for both positive and negative slewing signals. All that remains now, is to reinstate the input band limiting filter. On a power amplifier, a good rule of thumb is to set the -3 dB bandwidth to between 10 and 20 times the highest audio frequency – so somewhere between 200 kHz and 400 kHz. We will use 400 kHz in this case because it will be the worst-case condition and the most likely one in which to observe any undesired class B operating behaviour in the DB.

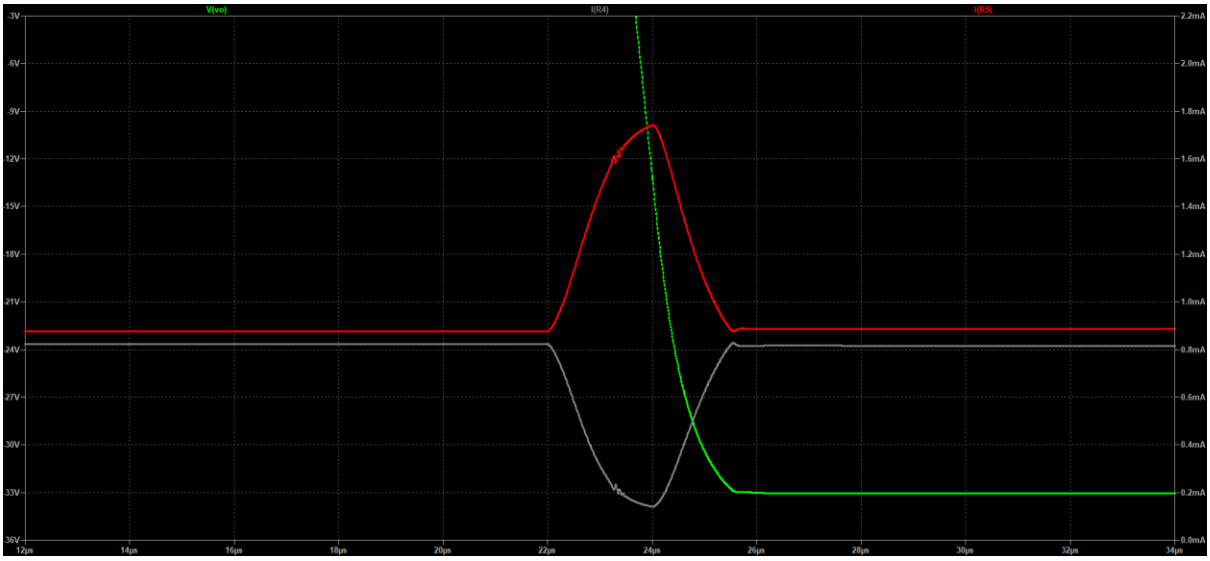

Figure 9 - DB response to worst case audio step signal with 400kHz input bandwidth limiting filter

In Fig. 9 above, under worst case conditions and an extremely conservative 2 us input signal source rise time, the current into the DB output summing junction remains in class A.

Insofar as the peak output current from the DB is concerned, this can be calculated by inspection by subtracting the peak feedback current fed in via Rf from the peak current fed in via R_{degen}. The resulting figure for the nx-Amplifier (and indeed the sx-Amplifier) is 8x the standing DB current of 1 mA, so ~8 mA peak which is confirmed through simulation.

It is important to note that this peak output current will only be delivered during full output *fast signal transitions*. During steady state sine wave signals and music signals, the DB output current will be very small since it is related to the change in input current to the TIS (an integrator, just like a VFA) multiplied by the loop gain to deliver the required output voltage to the loudspeaker: typically 10 uA peak to peak modulation on the DB standing quiescent current or there about as is clear from Fig. 5.

Summary and Conclusions

The tests conducted in the simulations examined the behaviour of a typical CFA DB front end under highly implausible operating conditions. Under these conditions, as would be the case with any competently designed VFA amplifier, it was possible to drive the CB such that with full scale step inputs, one half of the DB entered the non-conducting state – analogous to one half of a VFA input diff amp turning off in response to such a signal.

The input signal rise/fall time was then increased to 2 us and the DB remained in class A for both positive and negative slewing. Finally, the input signal bandwidth limited to 400 kHz to more closely emulate a wide bandwidth input filter on a high perfmance CFA amplifier and the DB remained in class A operation with a full-scale step input and holds true for any competently designed CFA DB input.

The claim that the DB stage on the input of a practical CFA audio amplifier operates in class B or class AB mode is thus incorrect.

Transients of this type will never be produced in any event from any audio signal source (CD, DAC, Tuner, Tape, phono etc). The behaviour wherein the front-end stage output current rapidly increases during very fast full-scale inputs to charge the compensation capacitor around the TIS (aka 'VAS') is similar to that of a VFA. In the VFA case, the correct design approach is to ensure that the front end *gm* is sufficiently low and that the input signal is suitably bandwidth limited (see the e-Amp write up for details on the approach in a high performance VFA). The front-end *gm* in a CFA is set by the feedback resistor value, so by selecting this appropriately during the design, linear operation of the amplifier loop is assured. Further, due to the 'current on demand' feature of the CFA topology, it is not possible to drive a CFA amplifier into slew limiting or for SID to arise during operation.

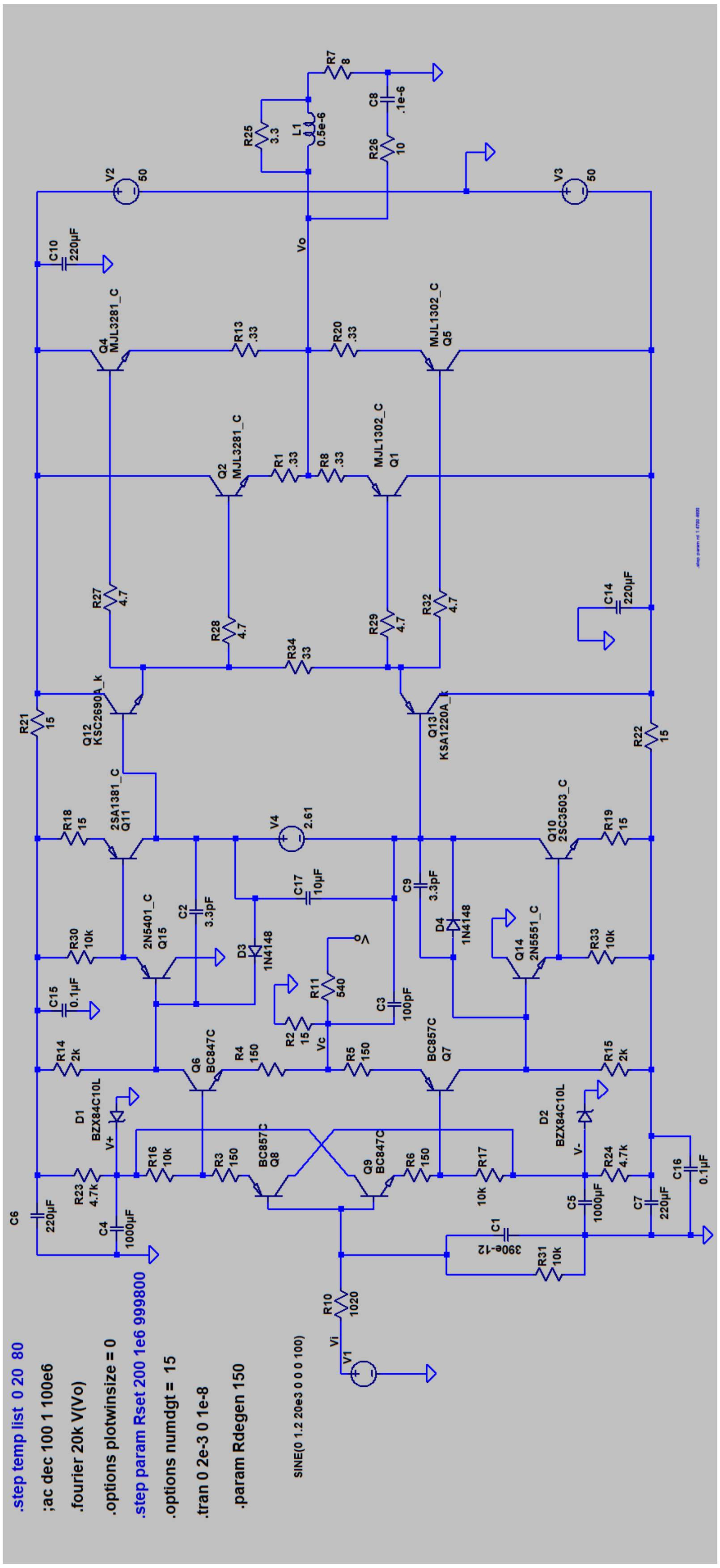

Figure 10 - nx-Amplifier LTSpice model

References

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