

Universal JFET Buffer

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A simple low distortion, wide bandwidth two transistor JFET buffer suitable for driving power equipping power amplifiers with volume controls or general purpose audio buffering.

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1. Introduction

A while back, one of the diyAudio forum members who was building the nx-Amp (here's [the thread](#) on DIYaudio.com) enquired about either reducing the amplifier's overall gain, or providing a volume control facility. Since both the 15 W class A [sx-Amp](#), and its bigger 100W sibling the [nx-Amp](#), are [Current Feedback Amplifiers](#), performance is quite carefully optimized for a specific gain – they are not as tolerant as voltage feedback amplifiers in this regard. Although not specifically raised in the thread, a consensus seem to develop that what was actually needed was a general purpose buffer that would accommodate the input from a pot, and be able to comfortably drive a power amplifier with typical input impedance of 10 k Ω .

I looked at a number of different configurations – see Fig. 1 – and finally settled on the simple current source loaded follower you see in Fig. 3.

No originality is claimed – Nelson Pass's B1 buffer has been around for years and is well regarded - the UBx 'Universal Buffer', as this will I hope come to be known, also uses this classic configuration (but without the cascode), which I believe was first published by either Siliconix or National Semiconductor way back in the late 1960's.

2. Specifications

General Description: Two transistor JFET buffer incorporating 10k log taper volume control for buffering and to equip power amplifiers with volume control facilities. Complete unit fits on a 25mm x 45mm PCB, including the Alps RK27 volume control potentiometer. This design uses SMD components.

Input Impedance	:10k (higher pot values may be used, but the noise and distortion performance will be affected)
Input Signal	: up to 8 V peak; nominal 1.5V pk, or 1V RMS
Gain	: 0dB
Volume Control element	: Alps RK27 Blue Velvet 10 k Ohm or 20 k Ohm Log taper (10k recommended)
Frequency Response	: 1.5 Hz to 10 MHz -3 dB : 20 Hz to 20 kHz -0.1 dB
Distortion	: Less than 10 ppm at 1V pk into 10 k Ω at 20 kHz : Less than 100 ppm at 5 V pk into 10 k Ω : distortion spectra all low order
Power Supply	: 21mA for both channels : can be powered from +-20 V through +- 70 V by adjusting value of on board dropper resistors – see text for details

3.Choices, choices . . .

Before we get into the detail of the UBx, lets look at other designs that were considered in Fig. 1 going from left to right.

JFET Basic Buffer. This design loads the source follower J6 with a two transistor current source. I looked at this since if you are able to adjust the current source easily, it provides a lot more flexibility in choosing the JFET follower. The distortion performance for this simple buffer is very good, given the circuit simplicity, topping out at about 25ppm at 5V peak into 10 k Ω .

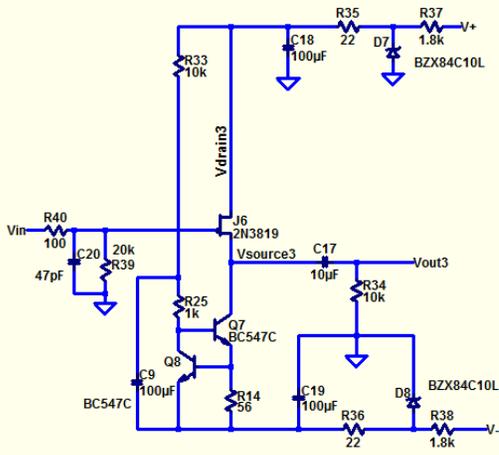
JFET with JFET Cascode. The JFET's input capacitance is modulated by the drain voltage, and to some extent its source, voltages. This gives rise to distortion, and one of the techniques here is to cascode the main amplifier or buffer JFET – in this case J3 is cascoding J2. This also improves PSRR, although in all of these circuits, it was very high (better than many op-amps at over 90 dB from LF through to 100 kHz) due in part to the action of the dropper resistors + filter capacitors in the supply rails. However, using this approach, you have to make sure that the cascade JFET (J3) Idss is HIGHER than the buffer JFET (J2) – if not, you are likely to encounter more distortion than necessary, as the follower JFET drain source current gets limited by the cascode device under heavy loads. I'll come back and discuss this a bit more with reference to the UBx. As with the first design, the simple bipolar transistor current source is retained.

JFET with Bipolar Cascode. This concept came about because I looked at avoiding the selection effort required for the casode JFET in the JFET cascode version above. Of course, you can also simply specify a JFET with a high Idss limit for this purpose. The bipolar cascode is cheap and easy to implement.

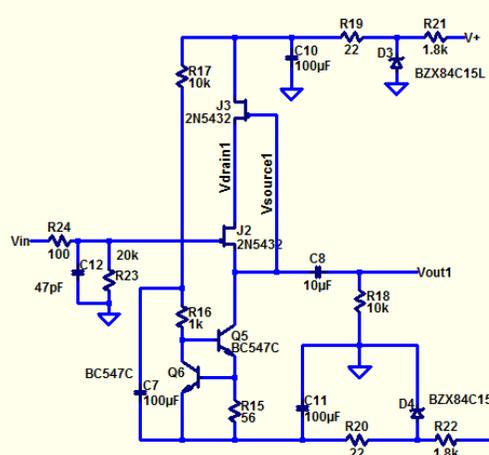
Reference Buffer with JFET Cascode. Similar to the first circuit, but with the bipolar current source replaced with a nearly ideal one.

In summary, all of these buffer circuits, despite their simplicity, displayed exemplary performance, with the highest only at around 10ppm at 2V into 10k (20kHz) and 25ppm at 5V pk into the same load. Further, and very importantly, the distortion spectra was all low order.

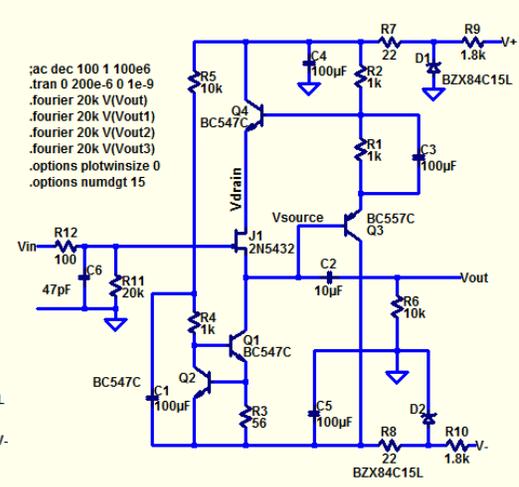
JFET Basic Buffer



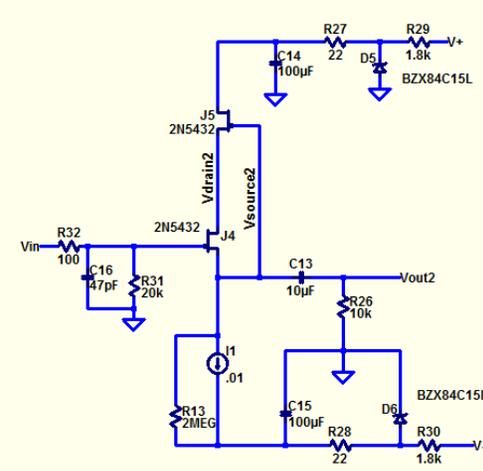
JFET with JFET Cascode



JFET with BIP Cascode

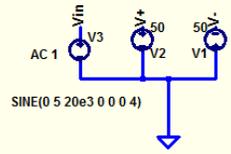


Reference Buffer



```

.ac dec 100 1 100e6
.tran 0 200e-6 0 1e-9
.fourier 20k V(Vout)
.fourier 20k V(Vout1)
.fourier 20k V(Vout2)
.fourier 20k V(Vout3)
.options plotwinsize 0
.options numdgt 15
    
```



Distortion - Upper figures 2 V pk into 10k at 20 kHz; lower figures for 5 V pk into 10k

0.001016%	0.000522%	0.000233%	0.000302%
0.002549%	0.001410%	0.017154%	0.000853%

Figure 1 Some Simple Buffer Topologies compared (results are all via LTspice simulation)

For the final circuit design, I went for a straight JFET current source loaded follower (Fig.2). I noted on sims, that using this simple buffer topology, low input capacitance JFETS gave remarkably good results: 1.5 V pk output at 20 kHz was < 10ppm, and the distortion spectra was 2nd with some 3rd and 4th only becoming apparent when the input was driven well beyond 2V pk output (see Fig. 4).

4. Circuit Description and Design Discussion (Fig 2)

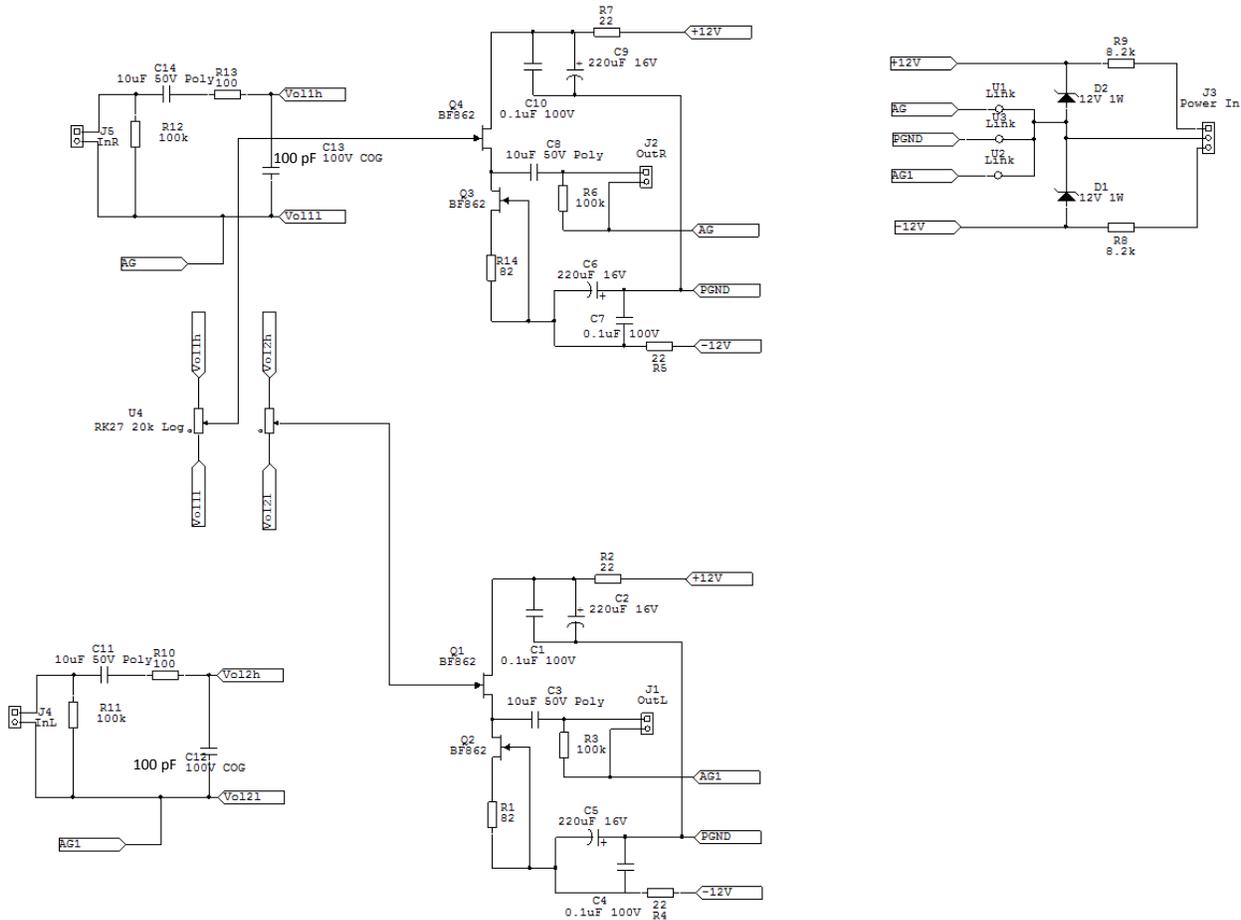


Figure 2 - UBx Circuit Diagram

We will cover the top half of the circuit which is the right channel. The input signal is fed in through a 2 pin connector (J5) with R12 providing a light load before feeding into the DC blocking cap C14, which then goes onto the HF filter comprising R13 (100 Ω) and C13 (100 pF) - this simply rolls off very high frequencies, since the buffer bandwidth is extremely wide. This buffer uses a 10 k Log taper [Alps RK27](#) potentiometer. These are good, general purpose pots which although not as good as a [discrete switched attenuator](#), nevertheless have stood the test of time and earned a solid reputation for reliability and good overall performance in the audio industry. You can pick these up from most of the big distributors and on ebay starting at about \$14. Note that you are not limited to the 10 k shown here

– its quite ok to go for a 20 k pot, or if needed 50 k or 100 k which you may want to do if feeding the UBx from a tube based preamp. Note however that with the higher pot values you need to consider the increased noise due to the higher source impedance and higher distortion (see below).

The pot wiper feeds directly into the [BF862 JFET](#) gate (Q4). These are made by NXP, and feature very low input capacitance, being originally designed for AM Radio applications, where this is an important parameter. They also happen to be quiet (typically about 0.8nV/√Hz at 100kHz, or 1uV of wideband noise¹ over a 20 kHz bandwidth), very cheap and readily available – when I looked, Mouser had about 20 000 in stock. Importantly, the I_{dss} spec on these devices is specified to lie between 10 and 20 mA, which means taking a worst case scenario, you can safely run the source load current at 5 or 6 mA, expecting a maximum of 4-5mA to be then available on the positive signal swings to flow into the load. I used the same device type for both the follower and current source.

I did some sims with high input capacitance JFETS, and for similar operating conditions, distortion was as much as 2 orders of magnitude greater than the BF862. Of course, as we saw from Fig 1., cascoding would all but cure this, but I really wanted to keep this buffer as simple as possible in order to make it compact and easy to build.

Q4's source is loaded with Q3, a simple JFET current source. This uses the same BF862 device, and R14 allows us to set Q3's drain current such that it falls below the lowest expected I_{dss} value for Q4. This is important because the total current (load and Q3 current) exiting Q4's source must be kept below the *minimum* I_{dss} value, which for the BF862 is specified at 10mA.

¹ Note that the 1/f however is not specified. Measurements made by various designers are around on the internet which seem to indicate that the device is well suited to audio – i.e. 1/f is sufficiently low enough not to be of any concern.

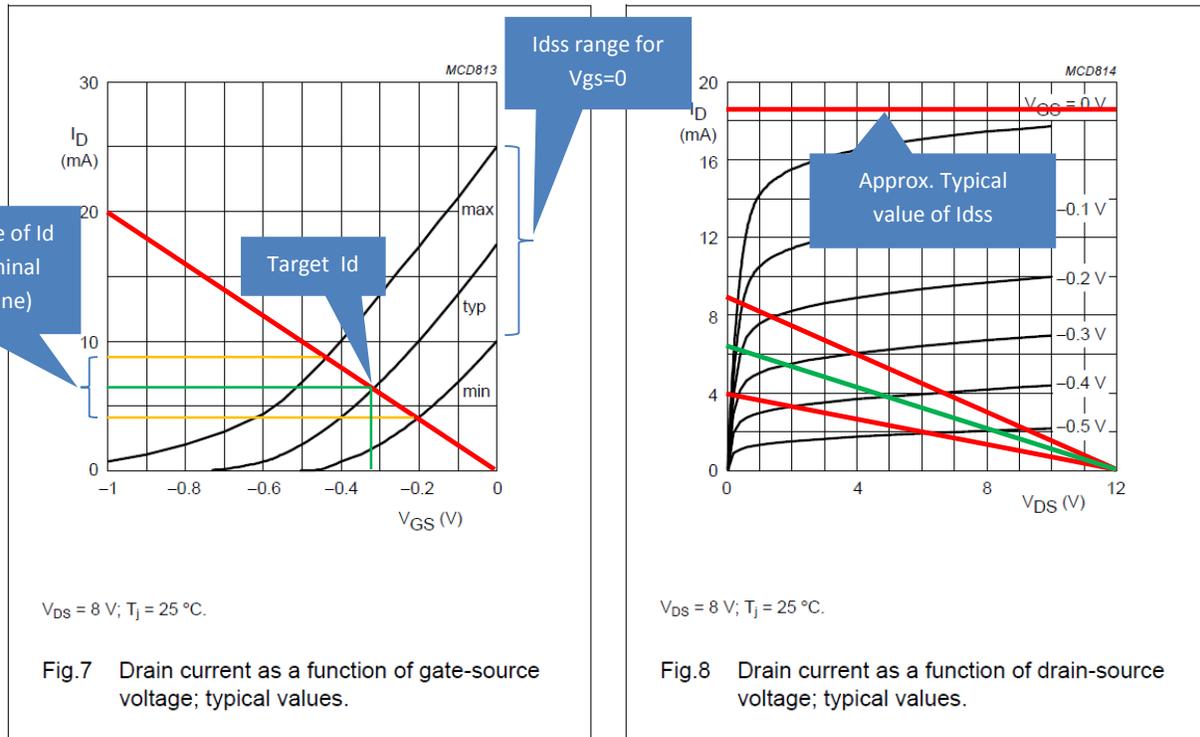


Figure 3 – NXP BF862 JFET Bias Curves: how to set the operating point

JFET Operating Conditions. Figure 3 is a snapshot of the BF862 bias curves from the [data sheet](#). Looking at the LHS panel, we see a set of 3 curves that prescribe the minimum and maximum variation in I_D vs V_{GS} . For our application, the maximum undistorted load current is 5V pk into 10k Ω – so 2mA. We also want to make sure that the maximum source current out of Q4 remains below the minimum I_{DSS} value of 10mA. If we then allow say 1mA to spare, this tells us the current source load needs to be somewhat below 7mA. Looking at the red line in the LHS panel, it can be seen that if we do not want to individually select the JFET's (i.e. just order them and place them on the board with a guaranteed good result) we have to ensure that at the upper I_D extreme (top curve in LHS panel), we do not exceed the I_{DSS} 10mA figure at 5V pk. Below that, we are ok, but have to accept that at >5V pk into 10k, there may be some additional distortion. 2Vpk will drive just about any power amplifier you can think of to full power and at that level, the distortion on this buffer is extremely low. We should conclude therefore that this is a sensible design tradeoff. Of course, you can always adjust the value of R1 and R14 individually to make sure that the current source is set to exactly 6.5mA – the target set above. With this information, its easy to now calculate the correct value of R1 and R14 from the typical curve from V_{GS}/I_D and we then get $0.32 \text{ V}/6.5 \text{ mA} = 49.2 \Omega$ – use 47 Ω standard value.

The output from the buffer is taken from Q4's source through another 10uF capacitor, with R6 providing some light output loading. It is possible to DC couple the output, but to do so would require tight matching of the JFET's (dual monolithics like the LSK489 would be ideal for this) and the addition of a resistor of the same value as R14 directly from the Q4's source to Q3. Some offset trim would still be required by adjusting the current source setting resistor (R1 and R14). However, since we want to be

able to have as few constraints as possible, including supply, this is not an approach pursued in this design.

DC blocking Capacitors. At this point you may ask why are DC blocking capacitors C11 and C14 necessary. Strictly, they aren't, and if your specific application does not need them, you can simply link them out on the PCB. However, cases may arise where you are feeding the buffer from a source that has a DC offset, and this is why they are included. Also, note that even with quite small DC offsets, you can get pot wiper noise, and these DC blocking capacitors prevent that as well.

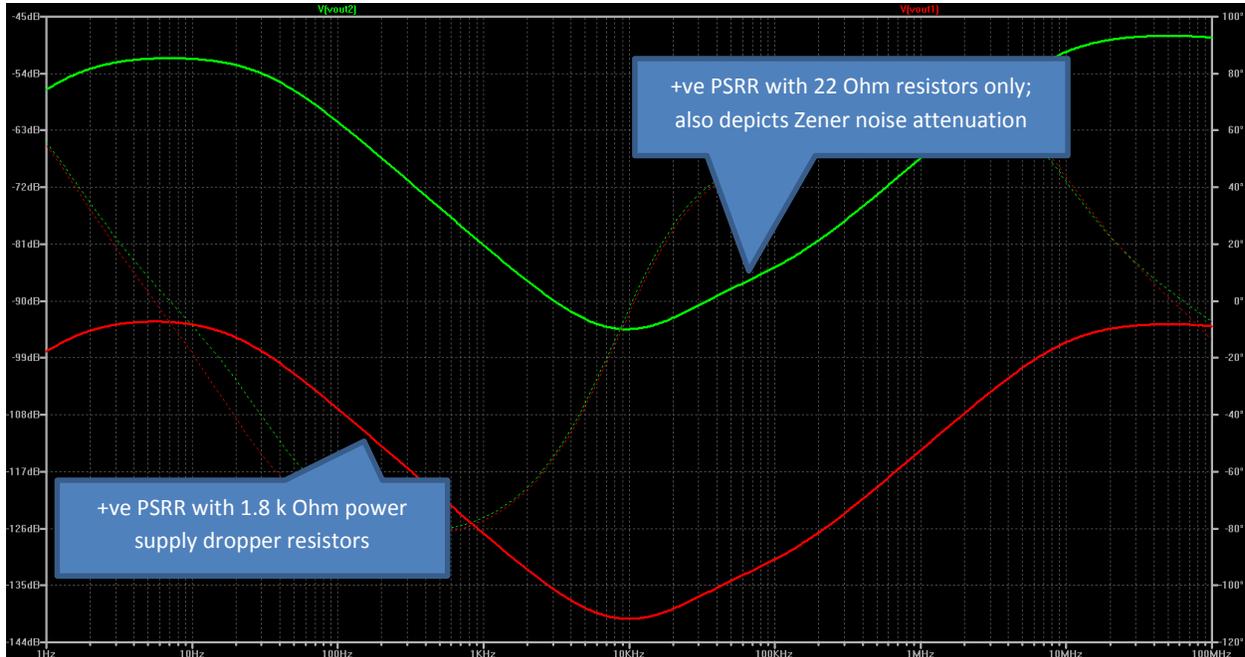


Figure 4 - +ve PSRR for the UBx Buffer. The -ve PSRR is considerably better out to about 500 kHz

Power Supply. Each rail within each channel is generously decoupled with a 22 Ohm and 220 uF capacitor. For rail noise and ripple, the dropper resistor also appears in series with the 22 Ohm filter resistor. The PSRR when using 1.8 k dropper resistors is shown in the red trace in Fig 4, while the green one depicts the performance with just the 22 Ohm filter resistors.

Some Zeners are noisy² and the 220uF decoupling capacitors in conjunction with the 0.1uF devices and the 22 Ohm resistor ensure this is attenuated – the green trace in Fig 3 approximating just the Zener noise attenuation. In practice, these overall PSRR performance figures are not attainable because of layout and other noise coupling mechanisms, but they do serve to show that an active voltage regulator to power the buffer is not needed – so, in keeping with my generally [minimalist philosophy](#) in life, the Zener regulators are my choice for this design. Fig 4 is for the +ve PSRR performance and the -ve rail

² See diyAudio member Christers LED and Zener [noise measurements](#). Note that above 6.8V, Zener noise tends to drop off considerably such that above 10V, wideband Zener noise is typically 2-3 uV - an easily manageable problem for such a simple regulator choice, and significantly better than an LM317/337 3 terminal device which is about 30uV/V where on a 15V output you can expect 450uV of wideband noise.

performance is *considerably better* beyond 10 kHz where it remains level at about 20 dB lower all the way out to 2 MHz, before rising. Note that I modeled the ESR of the capacitors at 100 milli Ω , based on typical 220 Ohm 35 V capacitor values and it is this which is responsible for the decrease in PSRR at HF, although drain-gate capacitance plays an increasing role here as well up at 1 MHz and beyond.

Distortion Performance. Fig. 5 shows the buffer FFT at 1V out into 10k Ω . The distortion is very low (\sim -100 dB) given the simplicity of the circuit, and the absence of feedback. Only at much high levels

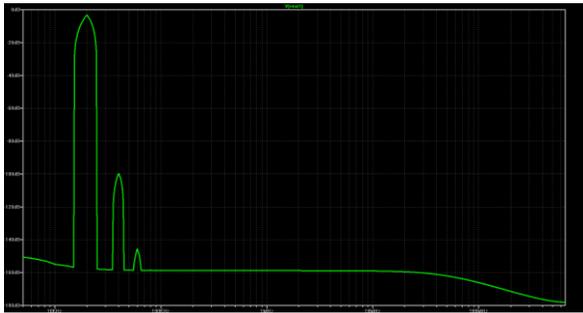


Figure 5 - UBx Distortion spectra at 1V into 10 k Ω (20 kHz)

and/or into heavier loads do you see thirds and 4ths

come up – importantly, there are no higher order harmonics, and this might tell us why a lot of well known audio designers like JFET's – the low order harmonics can be very euphonic, although at the levels I am talking about here (\sim 10 ppm at 1V output), you are not likely to hear them. Fig. 6 shows the distortion spectra at 5 V peak into a 10k Load –

again, all lower order harmonics, promising a smooth, fatigue free sound.



Figure 6 - UBx As in Fig. 5, but at 5 V into 10 K Ω (20 KHz)

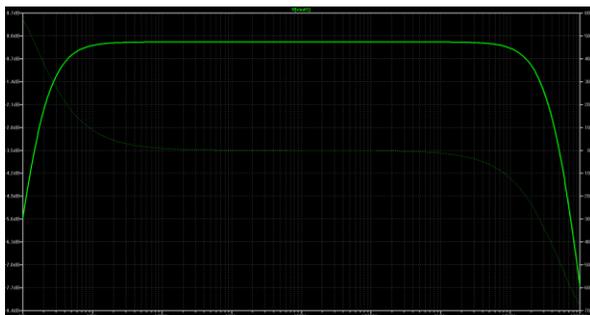


Figure 7 - UBx Frequency Response

Frequency response. Fig 6 shows the frequency response which is very flat over the audio band. The response without filtering extends all the way out to well above 50 MHz (sim). In practice its likely to be much lower than this; you can easily tailor the upper -3 dB to your requirement by adjusting the value of the input filter resistors R10 and R13 – raising these

to 1k for example will set the -3 dB frequency to about 5 MHz, although noise will be higher – the

other alternative of course is to increase the associated filter capacitors (C13 and C12).

5. Construction and Components

In order to keep the whole buffer compact, SMD devices are used where possible, ending up with a very tight PCB, including the Alps RK27 dual Gang pot, of about 25mm x 48mm (about 1" x 2") square. For the input coupling capacitors, I elected to go with film devices, since with electrolytics, there is a complete lack of consensus³ on their impact on the sound. However, because I needed a compact capacitor, I had to settle for a 10uF polyester type, which do suffer from distortion, but this is *only at high signal levels in the 5 to 10V RMS* range (see Douglas Self's 'Small Signal Audio Design for details) – there will be no impact on the performance at the signal levels we are talking about here. Remember, the buffer will typically be used up to about 1.5V peak output to drive almost any power amplifier to full power – at these levels, distortion is solidly under 15ppm into 10 k, and drops off rapidly below this. A polystyrene or polypropylene of similar value is about 3x the size and would require a much larger PCB. I made a reasonable tradeoff on this in my view.

The other TH components used were the two voltage dropper resistors, R8 and R9, to allow for up to 0.5W of total dissipation with an expected maximum current draw of 21mA, allowing for about 2.5mA of Zener current. If these are going to be running at near their maximum dissipation limit, I would stand them off the PCB by say 5mm so that they get more airflow around them for cooling purposes. Also note that there are 2W resistors available on Mouser in the same case size as general purpose metal film half watt devices that you may want to consider – just mount them with a gap between the resistor body and the PCB if dissipating close to 2 Watts.

It is very important that all of the 1206 SMD resistors used in this project are of the *thin metal film* type and NOT the common thick film variety. Again, turning to Self's 'Small Signal audio Design', you can see the plots of resistor non-linearity vs voltage, and thick film devices produce significant distortion – you must use metal film types. Here is a link to the type of device you need to use for reference, in this case the [Vishay commercial thin film P-NS](#). Note they are very low noise and specify the *voltage coefficient* <0.1ppm.

For the 220 uF capacitors, I have specified 6.3mm OD types. There are many manufacturers, but I suggest you use well known brands like Panasonic, Kemet etc.

³ DS view is just oversize them and the AP will show zero distortion' while JC avoids them at all costs, RC also does not like them and NP just encourages his followers to '... get over it' (i.e. their fear of 'lytics) ... I don't like them either for signal coupling – however, I used them in the e-Amp for DC blocking on the feedback and that amplifier sounds wonderful to my ears.