Ideas on Temperature Compensation for Emitter Follower Triples in Class AB Audio Amplifiers

This article discusses techniques for accurate and repeatable output stage quiescent current setting and stability on class AB amplifiers employing emitter follower triples (EFT). The shortcomings of the conventional two transistor voltage spreader circuit, also known as a Vbe multiplier, are explored, and a new approach, 'two point temperature compensation' proposed. A practical circuit is discussed, with simulation results, along with the effects on distortion performance in audio amplifiers using this technique.

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An enduring problem in audio amplifier engineering is that of temperature compensating class AB Emitter follower Triple output stages (EFT's). Let's size up the problem here, in bullet point format:-

- 6 base emitter junctions in series of c. 0.6V each at 25 C, for a nominal total of 3.6V
- An generally accepted temp coefficient of -2.2mV per C per base emitter junction, for a total stacked absolute temperature coefficient of -13.2mV per degree C
- The requirement to hold 52mV across the combined (i.e. negative and positive half) output stage emitter degeneration resistors – this for optimum distortion performance in class AB amplifiers – across the full expected operating temperature range of the amplifier

That's the basic requirement. Now let's look at the practical environment this has to work in, again, in bullet point format

- The output devices, driver and pre-driver transistor temperature coefficients are different because the current density's in the devices are different
- The pre-drivers, drivers and output devices are at different temperatures, this being very dependent on the heatsinking arrangements and pre-driver/driver nominal operating current levels, and the recent program material
- There is a significant temperature lag between the output device and the sensing device in the Vbe multiplier in conventional arrangements due to the variation in thermal mass between the various devices. For example, the thermal mass of the output devices on the heatsink is very high, whilst that of the pre-drivers, assuming free-standing mounting on the amplifier PCB, is low.

From the above, it's clear why this is such a difficult design problem – there are 3 independent variables (temperature coefficient – herein after termed 'tempco' - differences across the 6 devices, absolute temperature differences across the pre-driver, driver and output devices, and thermal inertia). The list of variables is not exhaustive, but these are the main ones.

Let us begin by taking a look at the conventional two transistor circuit, of which there are many variants[1].

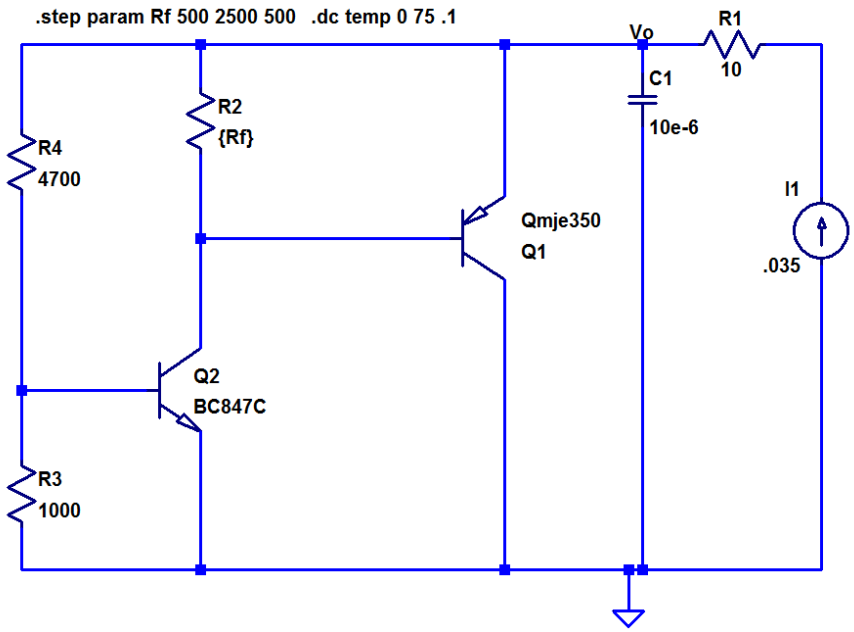

Figure 1 - Generic Two Transistor Vbe Multiplier

R3 and R4 set Vo, also known as the Vbe *multiplier, Vbe stand- off* or *bias spreader voltage* plus the output device emitter degeneration resistor bias voltage, which is 52mV[2] for a total of 3.652V (assuming a Vbe of 0.6V) for the EFT at 25deg C. In practice, there is significant variation around the spreader voltage part of this voltage stack at room temperature because it depends on the devices used and the standing currents through them. Normally, R3 is made adjustable, such that if the potentiometer wiper disconnects from the track for some reason, the Vbe multiplier back-off voltage goes down – i.e. it is failsafe.

Fig 2 shows a simulation result achieved by stepping Rf from 500 Ohms to 2500 Ohms. The tempco remains the same, whilst the stand-off voltage changes. If we hold Rf at some fixed value, say 1k Ohms, and vary R3 by an appropriate amount, then the stand-off voltage will change, and the tempco will also change.

[1] See Douglas Self 'Audio Power Amplifier Design Handbook' and Bob Cordell 'Designing Audio Power Amplifiers'

[2] The 52mV relates to the 26mV drop across each emitter degeneration resistor and is the value required for minimum distortion. Thus, across both the positive and negative half output stages, one has a total of 52mV

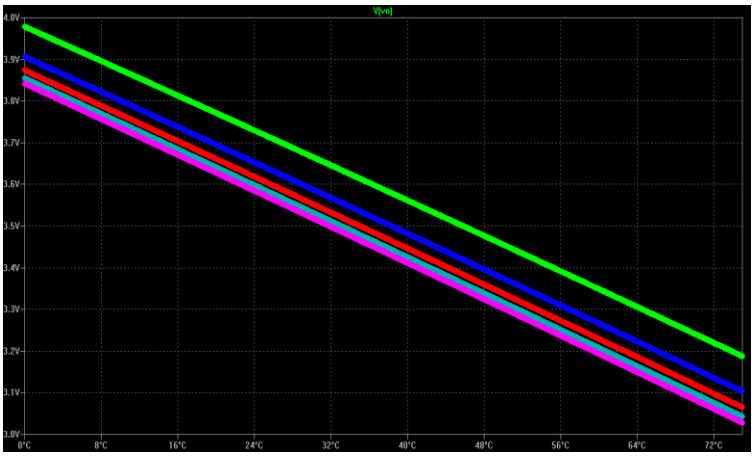

Figure 2 - Slope and Initial Spreader Voltage as a function of Rf

The temperature coefficient as measured between 0V and Vo is fixed by [(R4+R3/R3) * V_{TCO}], where V_{TCO} is the temperature coefficient of the base emitter voltage of Q2. This is conventionally taken as –2.2mV/C, but reality is somewhat different. V_{TCO} is highly dependent upon the device current density, and can be as low as 1.85mV/C which in the Fig 1 example gives an absolute tempco of –9.25mV/C. However, adjusting R3 also affects the tempco and the stand-off voltage. The standard spreader voltage circuit it can be concluded has a high degree of interaction between the stand-off voltage and the tempco due to the gain set by R3 and R4 and the sense transistor collector current. It therefore can only really provide optimum compensation over a narrow band of conditions, and set up is an exercise in compromise. I looked at a number of single, two and three transistor Vbe multiplier circuits from self and Cordell, and all suffer from the fact that the tempco slope and the stand-off voltage are highly interactive – none allow the tempco to be adjusted independently of the spreader voltage. This has resulted in a number of derivatives of this circuit being developed over the years which offer varying degrees of compensation, from as low as 40% up to 70% of the generally considered maximum of 6 x -2.2mV which is -5.28mV through to -9.25mV. The design methodology is to ascertain the system tempco and then select the circuit with the closest match - quite an empirical approach for such a critical function.

This leads on to thinking about the tempco problem differently: - What if the tempco could be set completely independently from the Vbe spreader voltage? The ideal Vbe EFT multiplier could then be specified as follows

1. Adjustable Vbe stand-off voltage – this to so we can set the EFT into forward bias so that there will be 52mV across the output stage degeneration resistors, plus a further 3.6 for the spreader voltage, assuming 0.6V per junction
2. Easily adjustable temperature coefficient. 6 Vbe junctions will have a nominal absolute temp coefficient of -13.2mV/C, assuming –2.2mV/C per Vbe junction. With a good design, we could allow for an adjustment range of say -6mV/C to -16mV/C across the entire 6Vbe stack
3. Fast sensor response time.
4. No thermal runaway – a critical design goal
5. Easy set up in the amplifier development phase – a simple procedure for quickly optimizing the thermal compensation design.
6. Zero or little interaction between the stand-off voltage adjustment and the tempco adjustment

In an ideal situation, all the EFT base emitter voltages would be known instantly and the Iq (this is the quiescent current through the output stage devices) adjusted to maintain the optimum bias point.

Traditional methods of ascertaining the output stage junction temperatures usually use a TO-92 or TO-126 device that is mounted on the main heatsink, or on top of one of the output devices. The thermal lags involved in this type of arrangement are significant and very sub-optimal and if you look at the distortion vs. time plot in Douglas Self's 'Audio Amplifier Design Handbook' it's clear that after a significant change in heatsink temperature, you are left with minutes of, or worse, of over or under bias and the result is unnecessary distortion.

Fig3 shows in graphical form how a system with independent adjustment of Vbe stand-off voltage and tempco adjustment, *two point temperature compensation* would work, while Fig 4 shows the error profile. At 25C, Vbe is set for the ideal Iq bias point which is 52mV across the emitter degeneration resistors – this is the 25C Iq intercept point or pivot voltage. Below this point, and dependent of the electrical and thermal specifics of the design, the compensation will deviate from the ideal down to the minimum rated operating temperature in either a positive (over bias) or negative (under bias) direction. It's unlikely that an amplifier will remain at 0C operating temperature, but this may be the situation at power-up and that's why it's important to design for this case. Above the 25C adjustment point, the amplifier also deviates from ideal, and the maximum deviation is set by the variables mentioned earlier on in this document. Looking at Fig 4, at the upper temperature Iq intercept point (shown at 55C in this example), the bias error will again converge on the optimum bias point, before diverging again at higher temperatures.

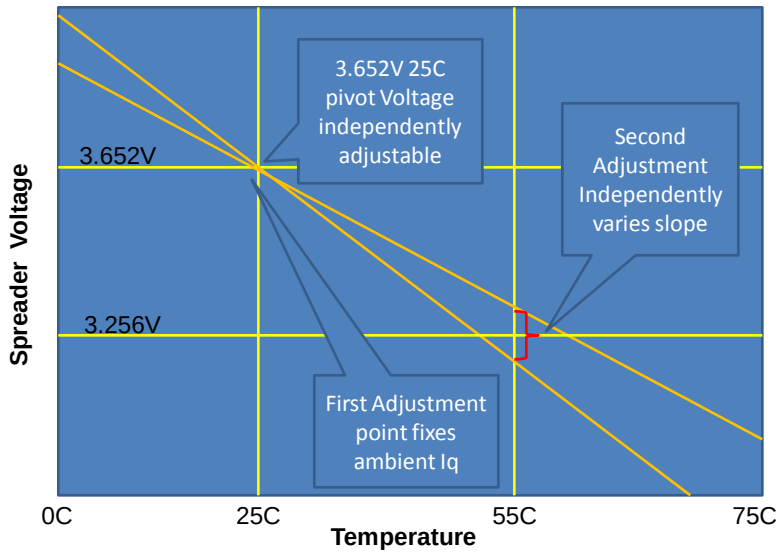

Figure 3 - Two Point Temperature Compensation

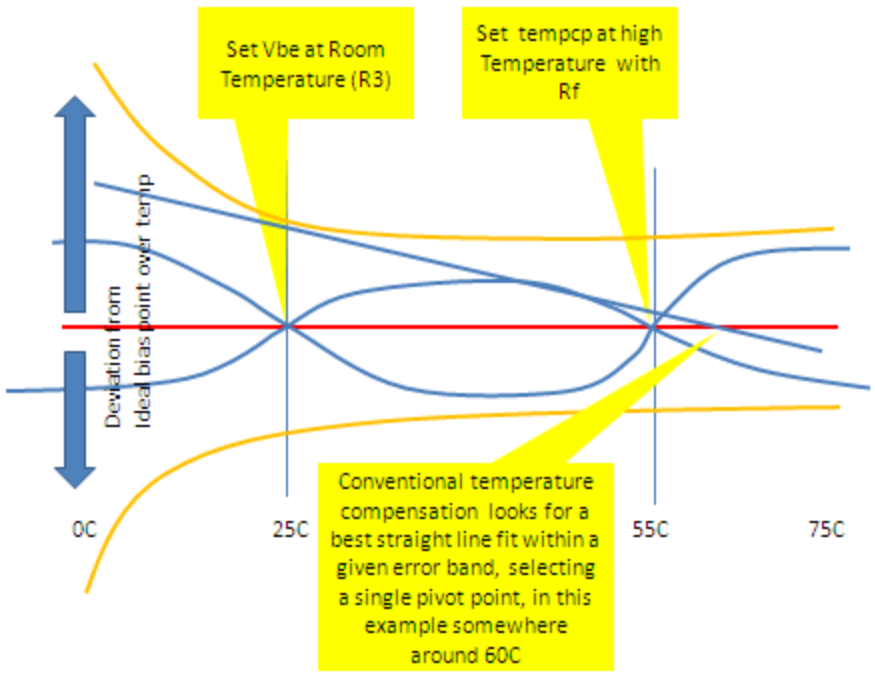

Figure 4 - Two Point Temperature Compensation Error Profile

Fig 5 shows some possible Iq vs. temperature profiles and we will use this to discuss some general points about two point thermal compensation. The x axis represents temperature and the y axis the deviation from ideal in these diagrams. The further the Iq line deviates from the red line, the higher the output stage distortion. Thus, for best performance, a perfectly compensated amplifier, Iq would remain steady over the full anticipated operating temperature of the amplifier and its heatsink – assumed in this discussion to lie from 0C through to 70C. The example black profiles in Fig 4 have been mirrored and drawn in orange to indicate that the bias error can be positive or negative. Again, it must be emphasized that these are example plots intended to aid in discussion.

In the first plot, Fig 5.1 we see that the initial bias point has been set to 25C and as in Fig 3 the error increases as temperature increases, and then curves back to meet the ideal Iq at 50C, before deviating again with further temperature increases into over bias. Below 25C, the amplifier is in under bias. Fig 5.2 shows another example, where Iq is correct at 25C and 50C, and the Iq error at other temperatures is always in over bias. Fig 5.4 shows the condition where an attempt has been made to set Iq with a single slope – the black and orange lines

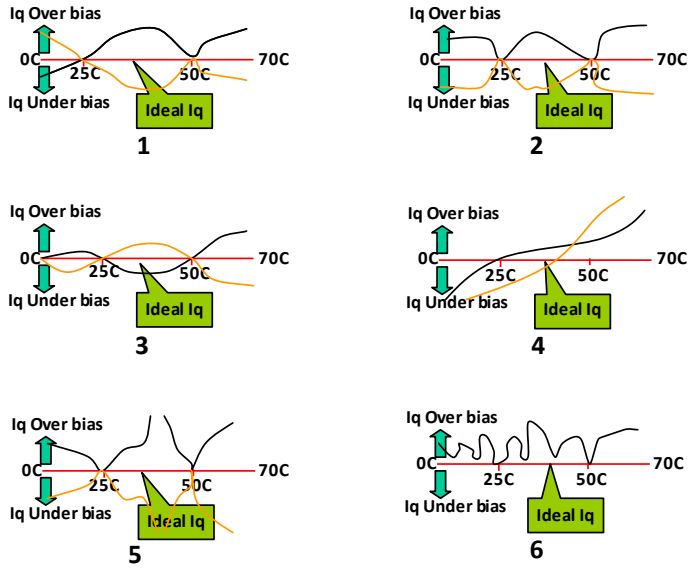

Figure 5 - Error Temperature Profiles

simply being two examples. Other than at the point where Iq intersects the red, ideal Iq value, the output stage is always either over biased or under biased. In a real world case, Iq would probably be set to ensure there was no thermal runaway at the upper end of the temperature range. Fig 5.5 shows the situation where there is a perhaps a grossly undersized heatsink, such that the amplifier goes into thermal runaway between 25C, where the initial Vbe multiplier voltage was set, and the higher temperatures, but before the 50C point. I have included this, plot because it does highlight that there may be higher than desired excursions in Iq away from the ideal in some cases, and this would be the situation, for example, where the drivers and pre-drivers were freestanding, not adequately heatsinked and got very hot. Other than providing more cooling, the best way to compensate for this is to move the initial Vbe spreader setup and the slope adjustment temperature closer together, making sure of course that at the temperature extremes, the error is still within satisfactory bounds. Finally, Fig 5.6 shows another example where thermal lags in the system and differing temperatures across the EFT transistors create multiple error nulls across the operating temperature range. If you look at the distortion vs. temperature plot in Self, it indeed shows this type of profile.

Two Point Temperature Compensation Circuit Techniques

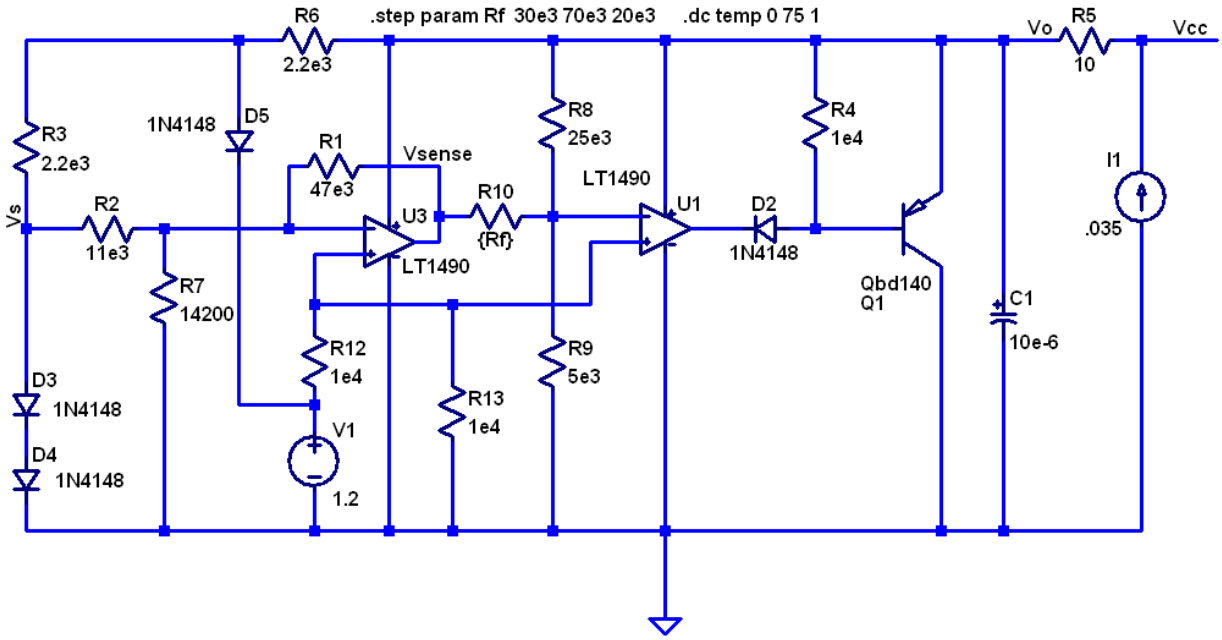

Figure 6 – Two Point EFT Vbe Spreader

For a little more complexity, and cost, it is very easy to design a circuit that easily fulfills the requirement to separate the Vbe stand-off voltage from the tempco adjustment – i.e. two point temperature compensation. Fig 6 shows a Vbe spreader based on a dual low voltage op-amp (LT1490, although almost any dual low voltage, low power rail to rail I/O op-amp will do) and a low cost 1.2V micro-power reference diode (e.g. LM385-1.2). This approach is more expensive clearly than the two transistor circuit, but it offers some distinct advantages.

The Fig 6 circuit consists of a shunt regulator formed by U1, V1 (an LM385-1.2 reference), Q1 and R9 and R8 plus D2 and R4. U3 and associated components form a temperature measurement circuit, with D3 and D4 forming the sensor elements (you could use a BAV99 dual diode in this position as well). D5 is simply used to provide an additional +0.6V standoff voltage to D3 and D4, thereby reducing substantially the change in current through the diodes as Vo changes. A current source drive to D3 and D4 would be ideal here, but this adds complexity that is not required. The ratio of R2 to R1 sets the gain of the temperature measurement circuit, and the output feeds into the shunt regulator feedback node at U1's inverting input via R6. R7 is used to extract a fixed current out of U3's inverting input summing junction, such that at the selected ambient temperature (typically 25C to 27C), Vsense (output of U3) is at the same voltage as that at the non-inverting inputs of the two op-amps – in this implementation, V1/2, or

0.6V. With this arrangement, as the temperature deviates either above or below ambient, the feedback node at U1's inverting input is pulled up or down, altering Vo accordingly. R10 sets the slope of the output voltage of the temperature measurement circuit, and as can be seen in Fig 6, this is made to vary from c. -6mV/C through to -16mV/C as R10 is changed from 70k down 30k.

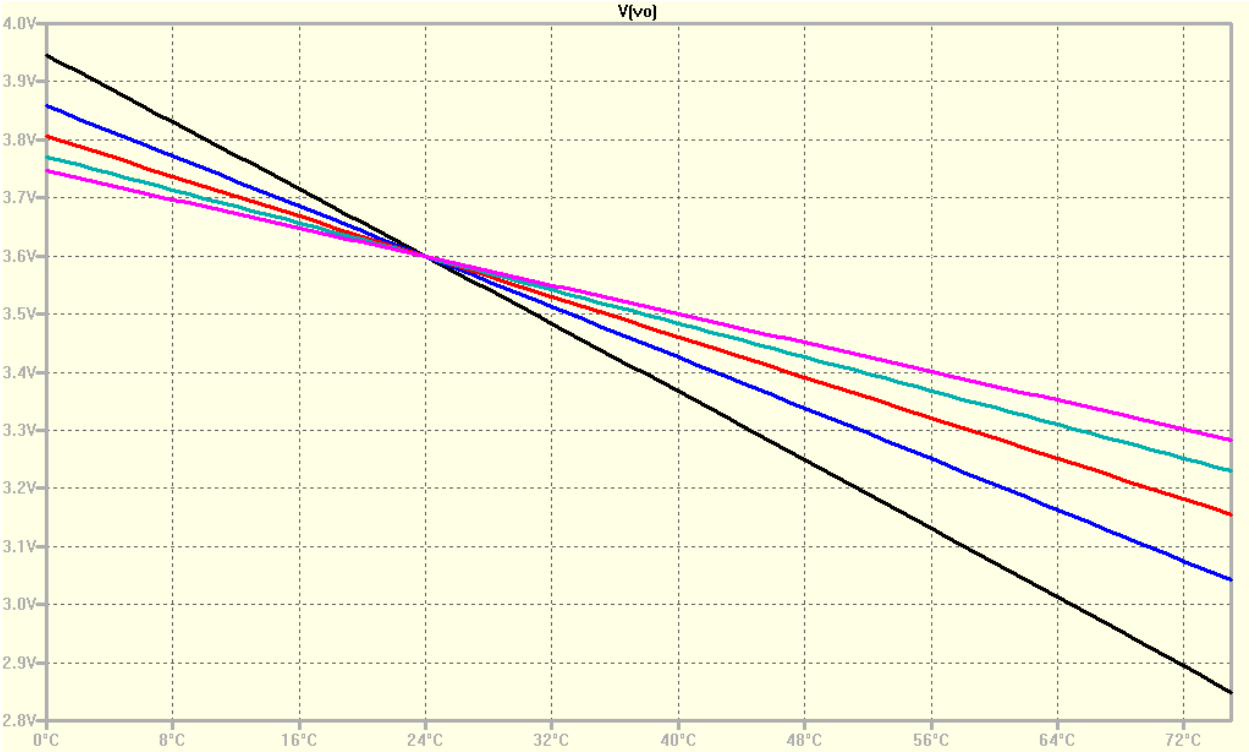

Figure 7 - Slope Range for the Circuit in Fig 6 (for simplicity, Vnom at 25C is shown as 3.6V and not 3.652V)

During the amplifier development stage, the initial Vbe set voltage (3.652V) is adjusted by trimming R9 at ambient. This should be done with R10 open – i.e. not connected to the junction of R9 and R8. The output of U3 at ambient should be the same voltage as the voltage at the non-inverting inputs to U1 and U3. During the prototype stage, this may necessitate some trimming of R7 to ensure this. *Critically, this sets the zero tempco point for the circuit at ambient*, and this can be seen in Fig 6, where the tempco lines all intersect at c. 24C. If for some reason your heatsink is sitting at 35C when you make this adjustment, all your tempco lines will pivot around this 35C point.

By adjusting RF during the prototype engineering phase anywhere between 30k and 70k, the circuit can be trimmed for the correct Iq tempco intercept point at the high temp calibrate point. The current draw of the control circuitry is around 2.5mA worst case. This circuits performance is very repeatable, and because of the high loop gain afforded by the op-amp, the output impedance is very low, thus easily catering for VAS standing currents anywhere between about 5mA all the way through to 40 or 50mA.

On Semiconductor NLJ3281/1302 devices incorporate a thermal sensing diode within the device package, and using a pair of this diode to make up the sensor diode (D3 and D4 in Fig 6) can yield a very

high performance Vbe spreader that maintains the required 52mV across the output device emitter degeneration resistors over a very wide temperature range. A further option is to use D3 to measure the output device temperature, and D4 to measure the driver temperature, leaving only the pre-drivers unaccounted for. With careful layout and good coupling, the thermal lag can be reduced to seconds and the temperature error to low single digit figures. Fig 7 details the slope adjustment range of this circuit.

Fig 8 shows an alternative circuit using a TL431[3]. These are low cost ($0.4) shunt regulators with an internal 2.495V reference, and they operate with shunt current from around 1mA through to a max of 100mA, although due to dissipation limits, this kind of current can only be handled at low shunt voltages.

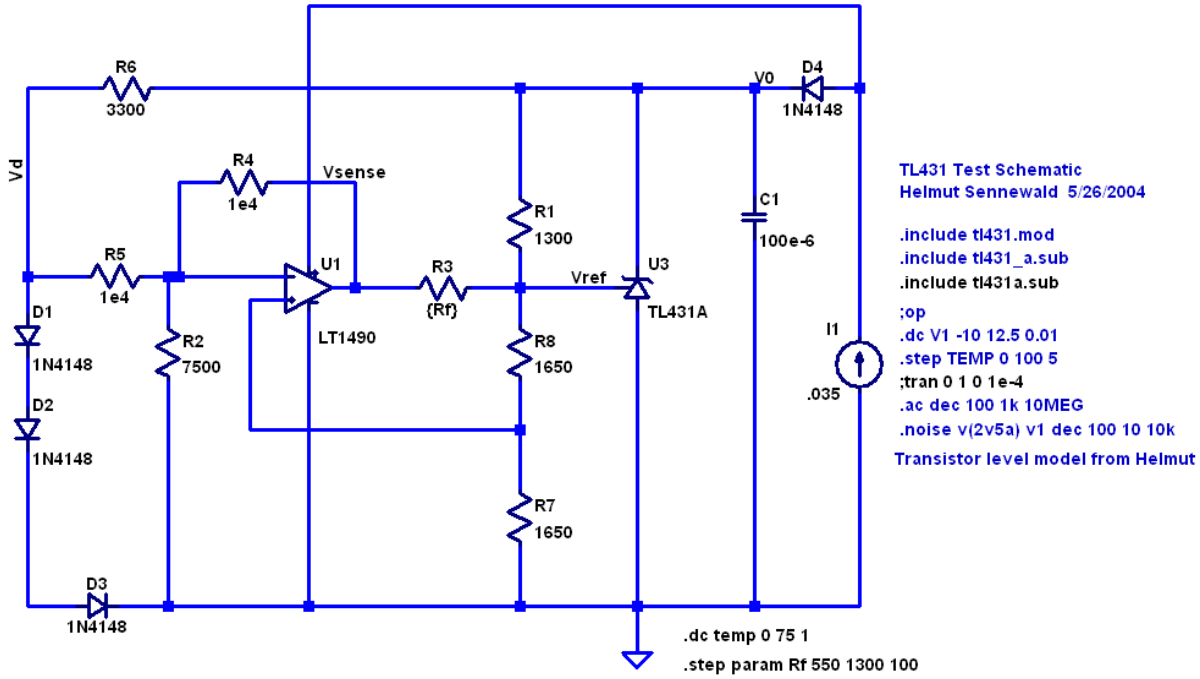

Figure 8 - TL431 Based EFT Bias Spreader

Using the TL431 saves on an op-amp, voltage reference, transistor and additional biasing components, making a much more compact, elegant design. Three diodes are used to sense the EFT transistor junction temperatures (D1 through D3) and this feeds into an inverting amplifier summing node configured around U1 via R5 with feedback provided by R4. R2 is used to offset U1's output (Vsense) to +2.5V to match that of the TL431 at 25C. It's important that this is set accurately as this then forms the 25C pivot voltage. The temperature gain slope of this circuit, which is of course –ve, is set by the value

[3] The TL431 model is by Helmut Sennawald, and is available on the LTSpice users group on Yahoo here :- TL431 LTSpice Model

of R3 – the lower, the greater the slope. The 1.25V reference for U1 is inferred from the input to the TL431 by means of R7 and R8, since this point must be at the same voltage as the internal TL431 reference.

Fig 9 shows the performance of the TL431 based EFT spreader. The pivot temperature is c. 26C and the slope can be varied independently by means of Rf from 6mV/C right through to 16.5mV/C.

The correct calibration procedure for this circuit, during the development phase of the amplifier, is as

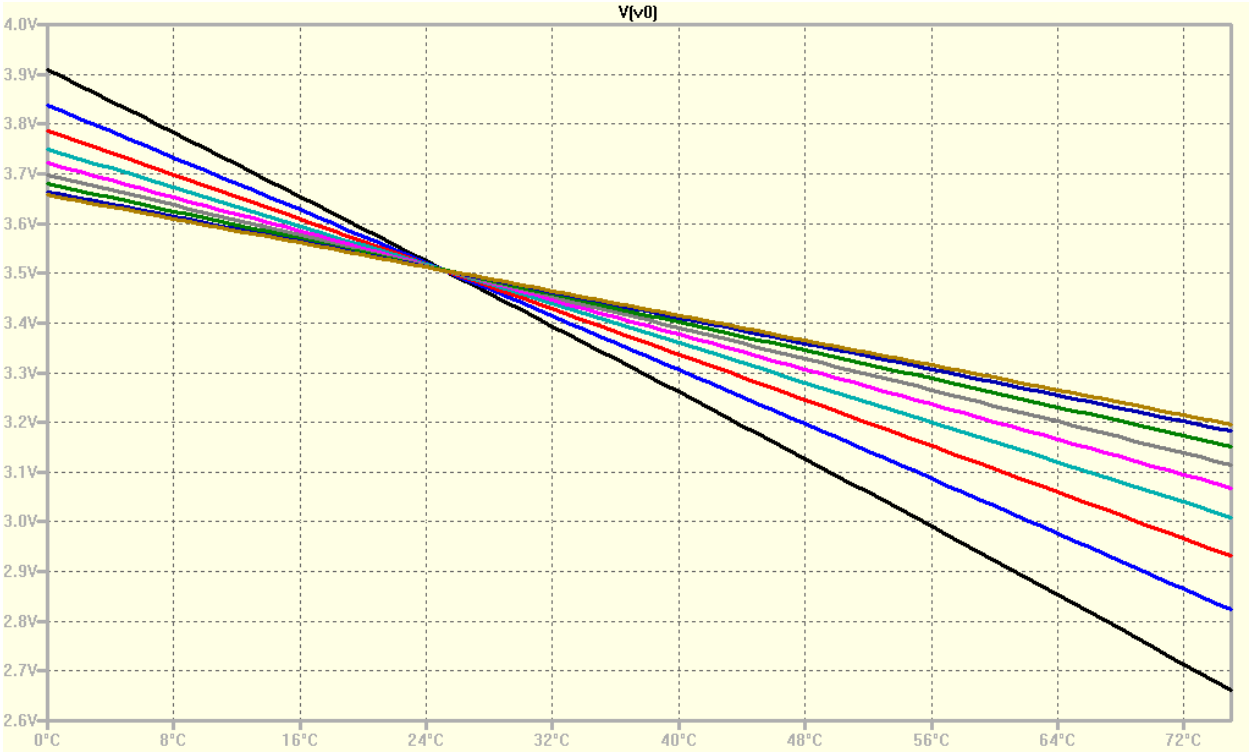

Figure 9 - Performance of TL431 Based EFT Spreader

follows:-

1. Disconnect Rf.
2. Measure Vsense wrt the cathode of U3– it should read 2.495V at 25C. If not, adjust R2 to obtain the correct value. This is best done by a parallel or series resistor combination, and it is important that it is set accurately - i.e. to within a few %. This sets the ambient temperature pivot voltage.
3. Next, set Rf to c. 800 Ohms. It is a good idea in the development phase to simply fit a 2k ten turn pot in place of Rf
4. At a nominal ambient temperature of 25C, adjust the pivot voltage by varying R1 such that the voltage drop across the output stage emitter degeneration resistors is exactly 52mV. This must be done with the junctions and heatsink at ambient, so it has to be done within a few seconds after power-up.

5. Next, drive the amplifier until the heatsink reaches 55C and settles at this temperature. If you need to, adjust the input signal to achieve this.

6. The amplifier Iq will probably be significantly different to that set at ambient, and thus the voltage drop across the emitter degeneration resistors will also no longer measure 52mV.

7. Now, at 55C adjust RF so that the voltage across the emitter degeneration resistors is 52mV.

8. RF can now be replaced with a fixed resistor, whose value is fixed for the thermal and mechanical design of the amplifier – no need to change it unless the heatsinking or type of transistors used in the amplifier output stage change.

For production, only the pivot voltage need be adjusted for the correct reading across the emitter degeneration resistors at ambient.

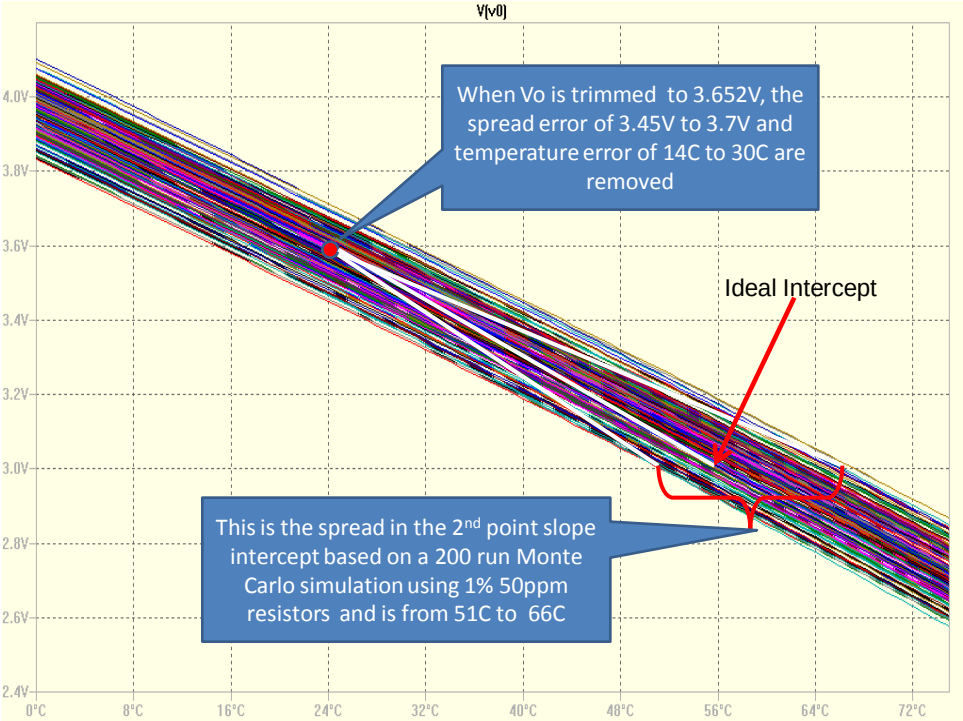

Figure 10 - Monte Carlo Analysis of TL431 EFT Vbe Spreader

Fig 10 details the results of a 200 run Monte Carlo analysis using 1% 50ppm resistors, and shows how the spread error affects the intercept point. If the error is dialed out at 25C, then the worst case circuit to circuit spread upper temperature intercept point, assuming Rf is fixed as in the design phase, is indicated by the red bracket and ranges between about 51C and 66C. This analysis has been included to indicate the expected performance of the circuit using standard tolerance components. If this spread is too great, and there is concern about thermal runaway at the upper temperature limit, the 2nd trim point (i.e. the upper temperature trim point) should be moved to a higher or lower temperature and this value used in production. Again, to make it clear, the advantage of two point temperature compensation is that once the slope is fixed during the

development phase for a given thermal and mechanical layout, only 1 adjustment at ambient is required – that to set up 52mV across the output stage emitter degeneration resistors.

It is also possible to reverse the procedure by firstly driving the amplifier until it is hot, then adjusting the spreader voltage so the correct 52mV is measured across the output device emitter degeneration resistors. The amplifier is then allowed to cool, and the slope adjusted at ambient so that the correct bias voltage is measured across the output stage degeneration resistors. This approach however, is not as production friendly.

For the practical execution of the above circuit, the ideal temperature sensor is a diode closely coupled to the output device chip, as in the On Semiconductor NJL3281/1302 devices. Using the circuit in Fig 8, D3 say, could represent one of the output device diodes. For the pre-driver and driver, the sense 1N4148 diodes should be placed close to the device collector leads and thermally coupled to them using a small amount of heatsink compound – these would be D1 and D2 (its quite permissible to change the order of the diodes). It's important here to keep the thermal inertia low so that the diodes quickly track the transistor die temperatures. It's for this reason as well that if at all possible, SMD diodes should be used. On a bipolar transistor, the collector is connected to the copper header inside the device, so if you can determine the deader temperature, you have a pretty good idea about the die temperature.

If your design does not use the On Semiconductor output devices, using a 1N4148 diode to measure the output device die temperature can also be done as indicated above. I have tried this technique and it works remarkably well on power devices, probably because the big thick collector lead is a good heat conductor.

Further developments

Moving forward, there is the option of using a small uC (8 pin 8 bit device) to digitally correct the 1st order correction provided by a simple one or two transistor Vbe spreader as shown in Fig 1, or a simple TL431 based fixed voltage shunt regulator. This then raises the prospect of being able to apply feed forward correction to compensate for the thermal time lags, thereby dynamically reducing system Vbe multiplier errors, possibly limiting the total tracking error to just a few degrees across the full operating temperature range of the amplifier. Feed forward techniques and self calibration offer the opportunity to reduce the time-temperature error to a few 10s of second's worst case. However, that will have to remain the subject of a future article.